IN THE SPECIFICATION

Please change the title to – Stackable Semiconductor Package Having Semiconductor Chip Within Central Through Hole Of Substrate --.

Please insert the following header and paragraph at page 1, before the header "BACKGROUND OF THE INVENTION:"

CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a continuation of U.S. Patent Application Serial Number 09/774,952, filed on January 30, 2001, now Patent No. 6,762,078 which was a division of U.S. Patent Application Serial Number 09/574,541, which was filed on May 19, 2000, and issued as U.S. Patent Number 6,395,578 on May 28, 2002, to which priority is claimed.

Please insert the following new paragraph at page 11, line 10 before the paragraph beginning with "Figs. 6A and 6B are . . .":

Fig. 5A is a cross-sectional side view of a stack of two laminated semiconductor packages of Fig. 4.

Please amend the paragraph beginning at page 15, line 17 as follows:

The circuit pattern 18 formed on the second major surface 11b of the resin substrate 17 may also be provided with a plurality of ball lands 18b, as in a semiconductor package 104 illustrated in Fig. 4. As shown in Fig. 4, the ball lands 18b formed on the second major surface 11b of the resin substrate 17 are not covered with the cover coat 19 covering the associated circuit pattern 18 in such a fashion that they are open. This means that a plurality of semiconductor packages having the above mentioned structure can be laminated together. That is, the lamination of a number of semiconductor packages can be achieved under the condition in which a plurality of conductive balls 60 are additionally fused on the ball lands 18b formed at the second major surface 11b of the resin substrate 17 in the semiconductor package 105 of Fig. 5. An exemplary stack 1040 of such laminated (i.e., stacked) semiconductor packages 104 is illustrated Fig. 5A.